

FIGURE 1(a)

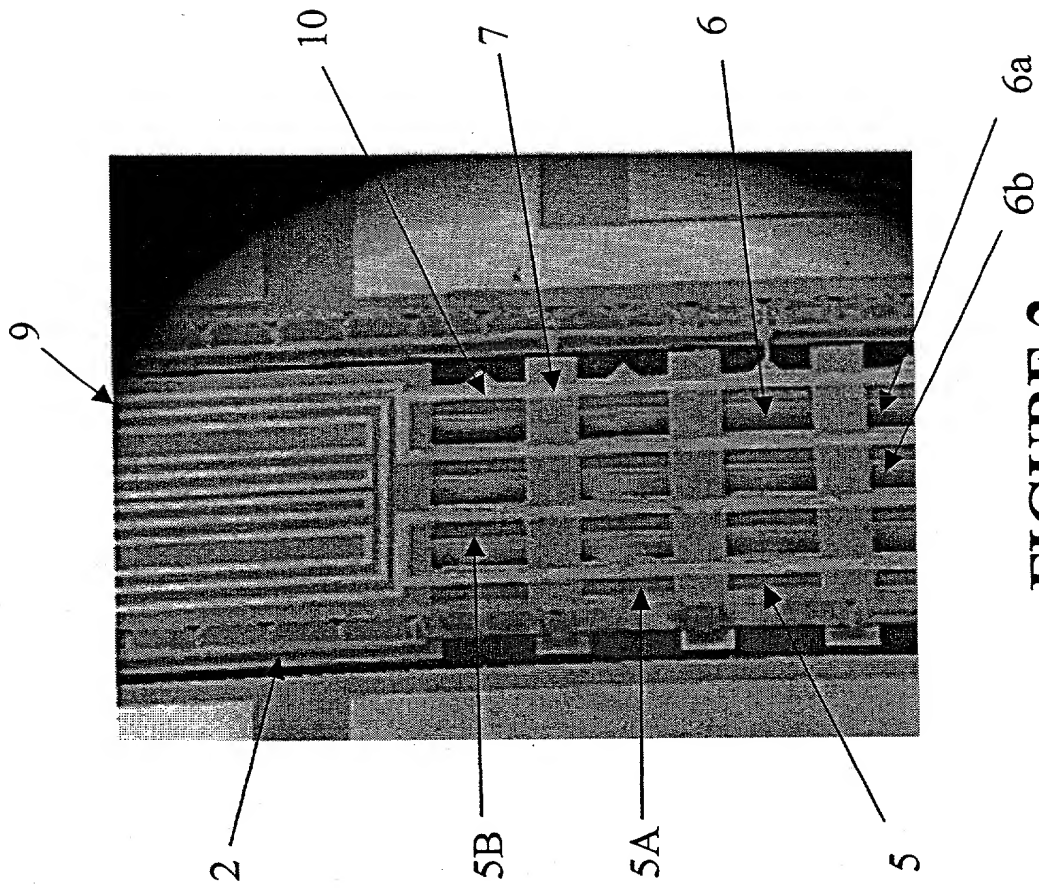


FIGURE 2

Small text block, likely a legend or reference, located in the upper left corner of the page.

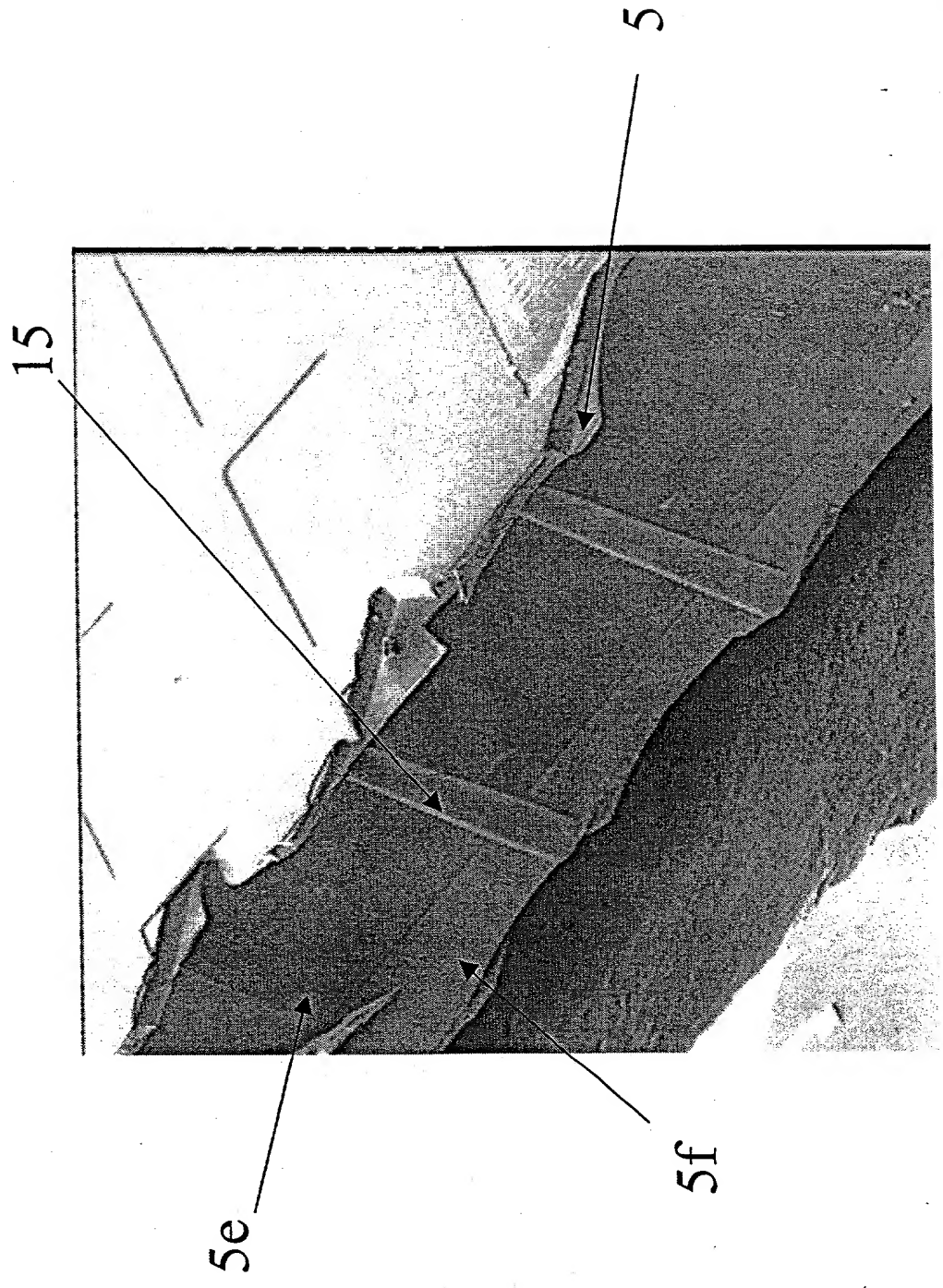
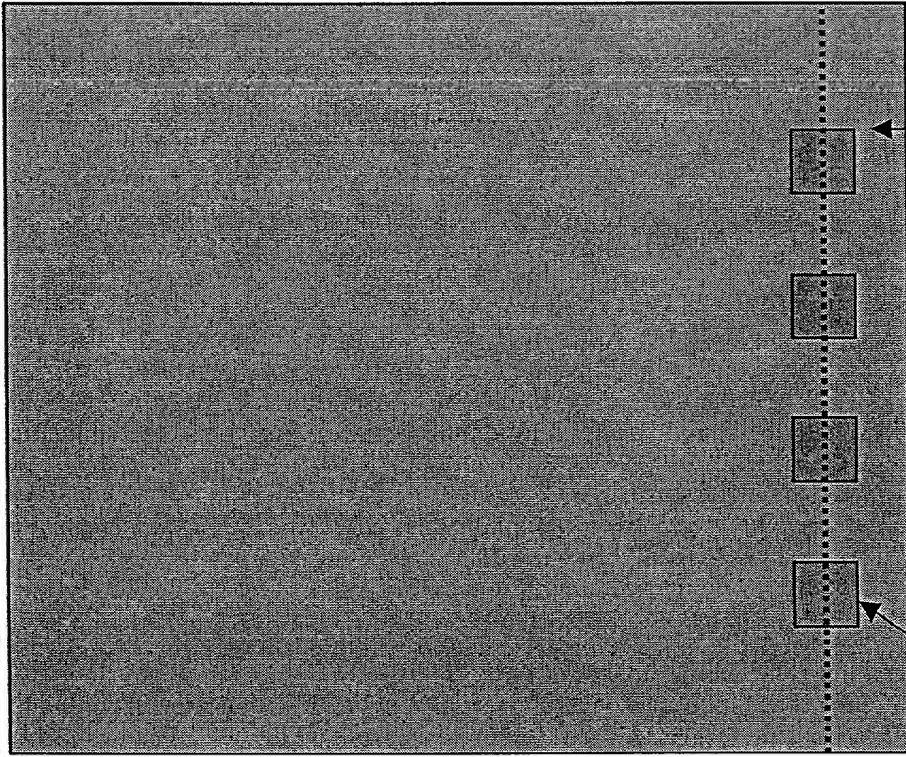


FIGURE 3

FIG. 5(a) is a schematic diagram of a device 100 in a first state. The device 100 includes a substrate 101, a first layer 102, a second layer 103, and a third layer 104. The first layer 102 is disposed on the substrate 101, and the second layer 103 is disposed on the first layer 102. The third layer 104 is disposed on the second layer 103. The first layer 102, the second layer 103, and the third layer 104 are disposed in a row. The first layer 102, the second layer 103, and the third layer 104 are disposed in a row. The first layer 102, the second layer 103, and the third layer 104 are disposed in a row.



104 **FIGURE 5(a)** 103

FIG. 5(b) is a cross-sectional view of a substrate 103 having a layer 104 of a material having a thickness of 400-500 μm. The layer 104 is formed on the substrate 103 by a method such as sputtering, CVD, or the like.

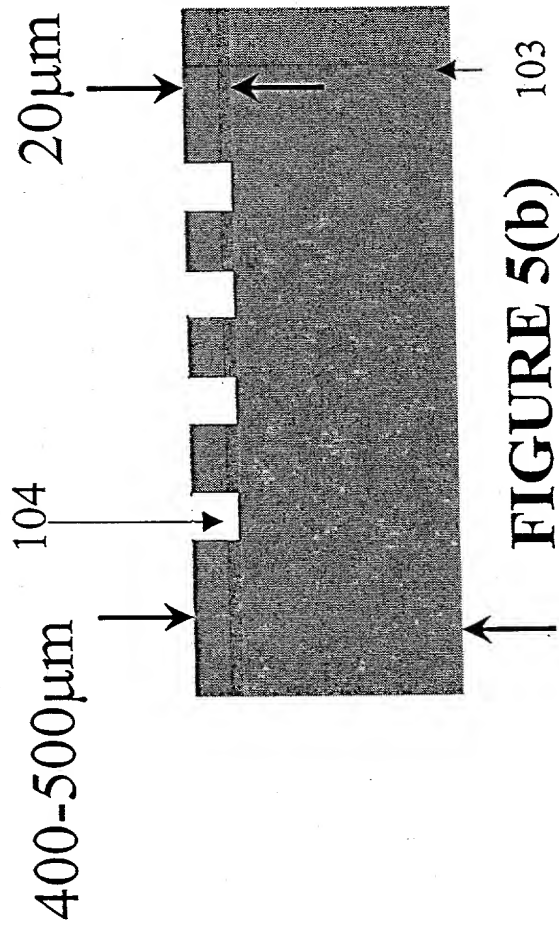


FIGURE 5(b)

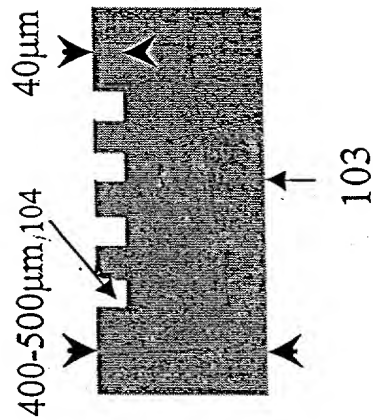


FIGURE 5(c)

FIG. 5(d) is a plan view of a semiconductor device in a fourth stage of manufacturing. The device includes a substrate 104 with a patterned layer 111. The patterned layer 111 is divided into four regions by vertical dashed lines labeled I, II, III, and IV. The regions are further divided into sub-regions labeled 120, 122, 135a, 136b, 140a, and 140b. The patterned layer 111 is formed by a series of rectangular blocks arranged in a grid. The regions I, II, III, and IV are separated by vertical dashed lines. The sub-regions 120, 122, 135a, 136b, 140a, and 140b are defined by horizontal and vertical dashed lines. The patterned layer 111 is formed by a series of rectangular blocks arranged in a grid. The regions I, II, III, and IV are separated by vertical dashed lines. The sub-regions 120, 122, 135a, 136b, 140a, and 140b are defined by horizontal and vertical dashed lines.

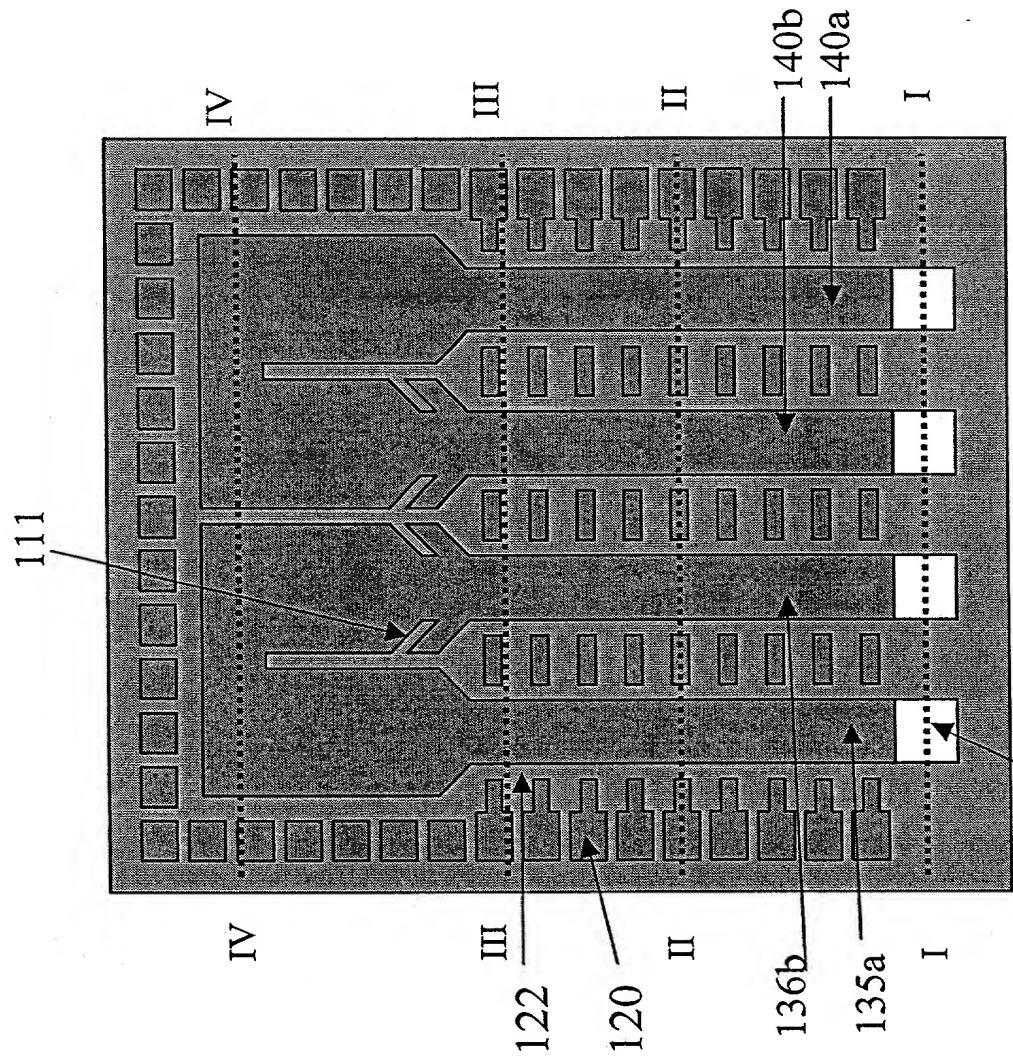


FIGURE 5(d)

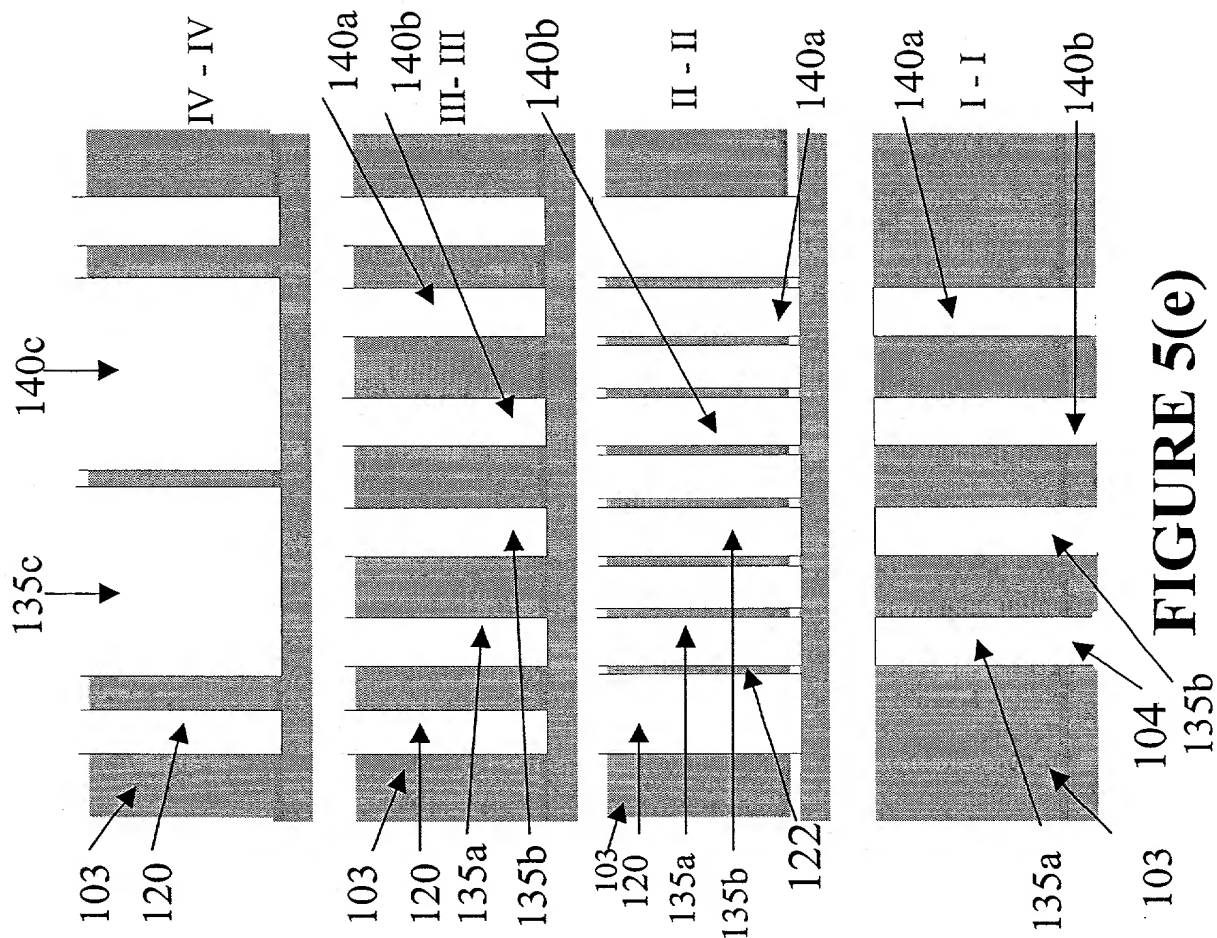


FIG. 5(g) is a perspective view of the third embodiment of the present invention, showing a cross-section of the device. The device includes a base 103, a top 125, and a side 130. The side 130 is formed by a series of vertical members 120, which are connected by horizontal members 135a and 135b. The top 125 is formed by a series of horizontal members 140a and 140b, which are connected by vertical members 140c. The device is shown in a perspective view, with the base 103 and top 125 being shaded to indicate depth.

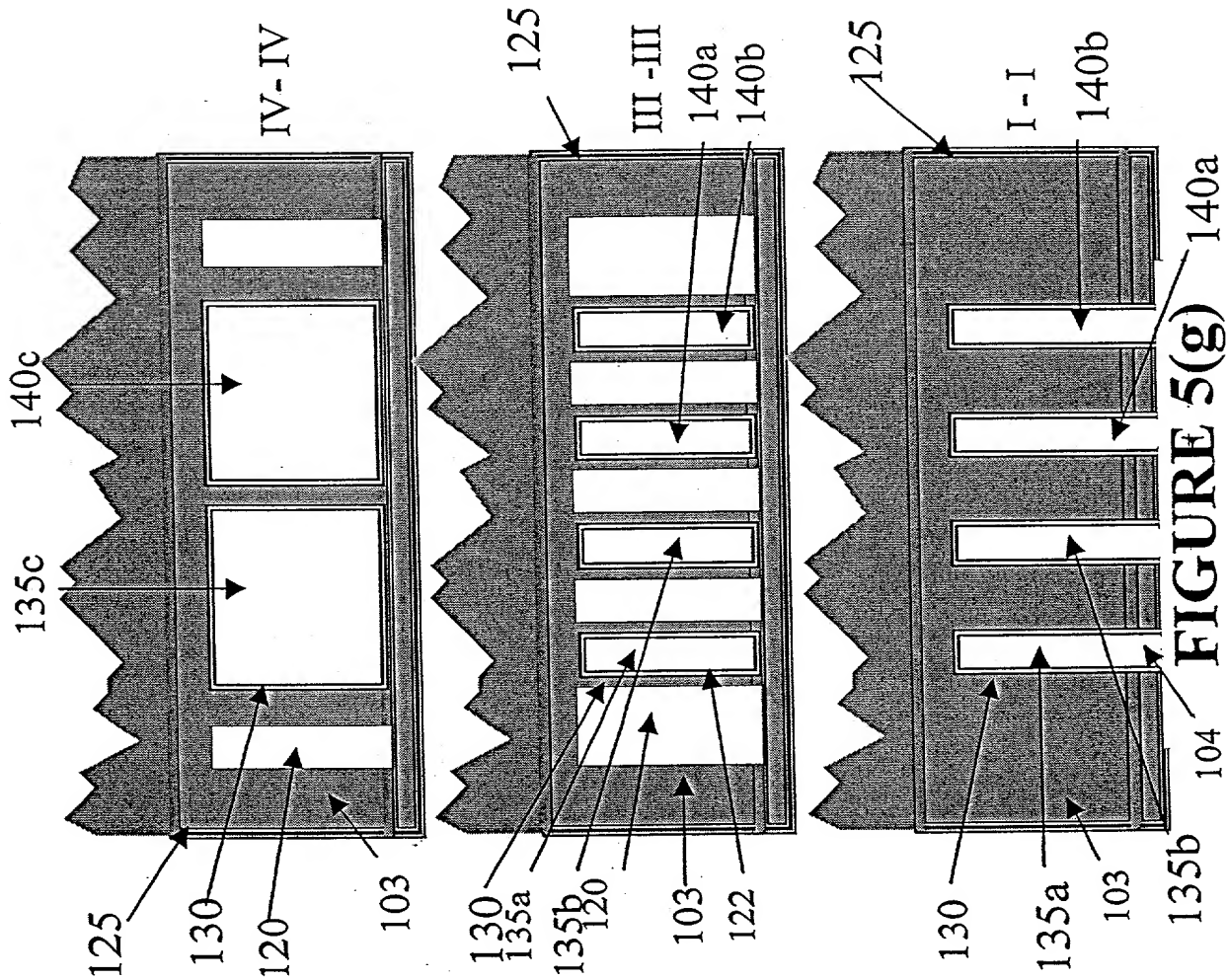
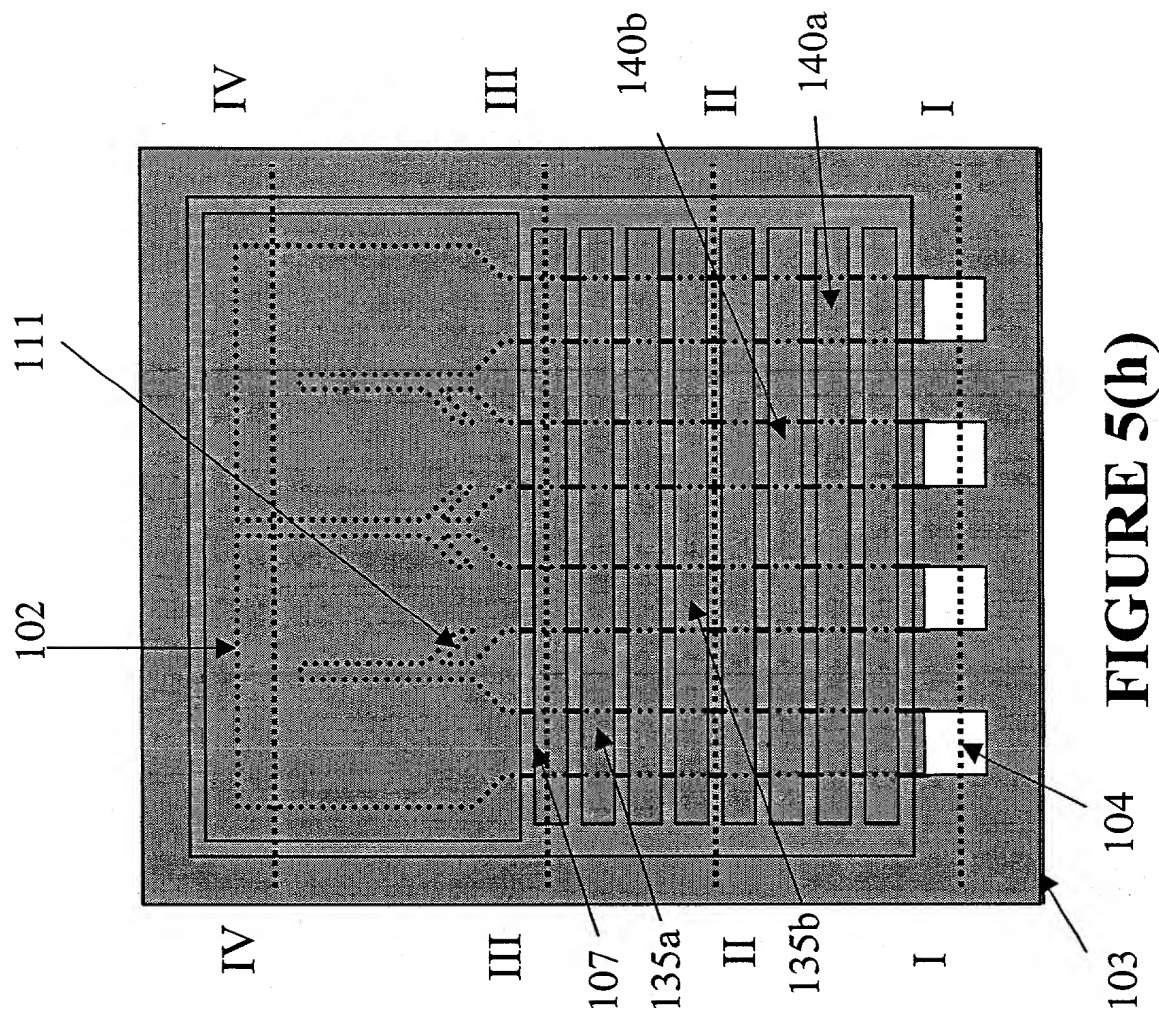


FIGURE 5(g)



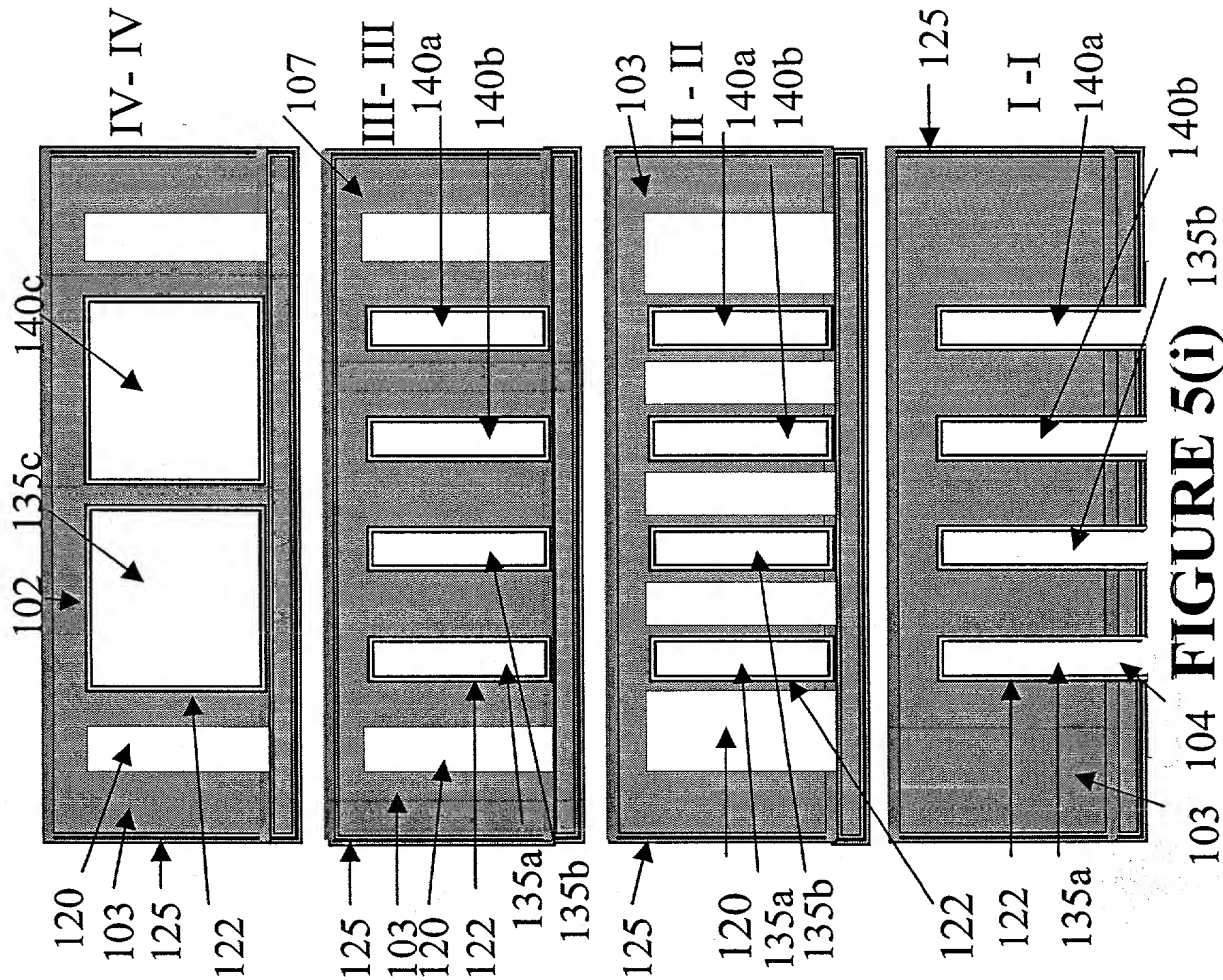


FIG. 5(j) is a schematic diagram of a device 100 in a perspective view. The device 100 includes a substrate 101, a gate dielectric layer 102, a gate electrode 103, a channel layer 104, a source/drain region 105, a gate insulating layer 106, and a passivation layer 107. The device 100 is a thin-film transistor (TFT) structure. The gate electrode 103 is formed on the substrate 101, and the gate dielectric layer 102 is formed on the gate electrode 103. The channel layer 104 is formed on the gate dielectric layer 102, and the source/drain region 105 is formed on the channel layer 104. The gate insulating layer 106 is formed on the channel layer 104, and the passivation layer 107 is formed on the gate insulating layer 106. The device 100 is a top-gate TFT structure.

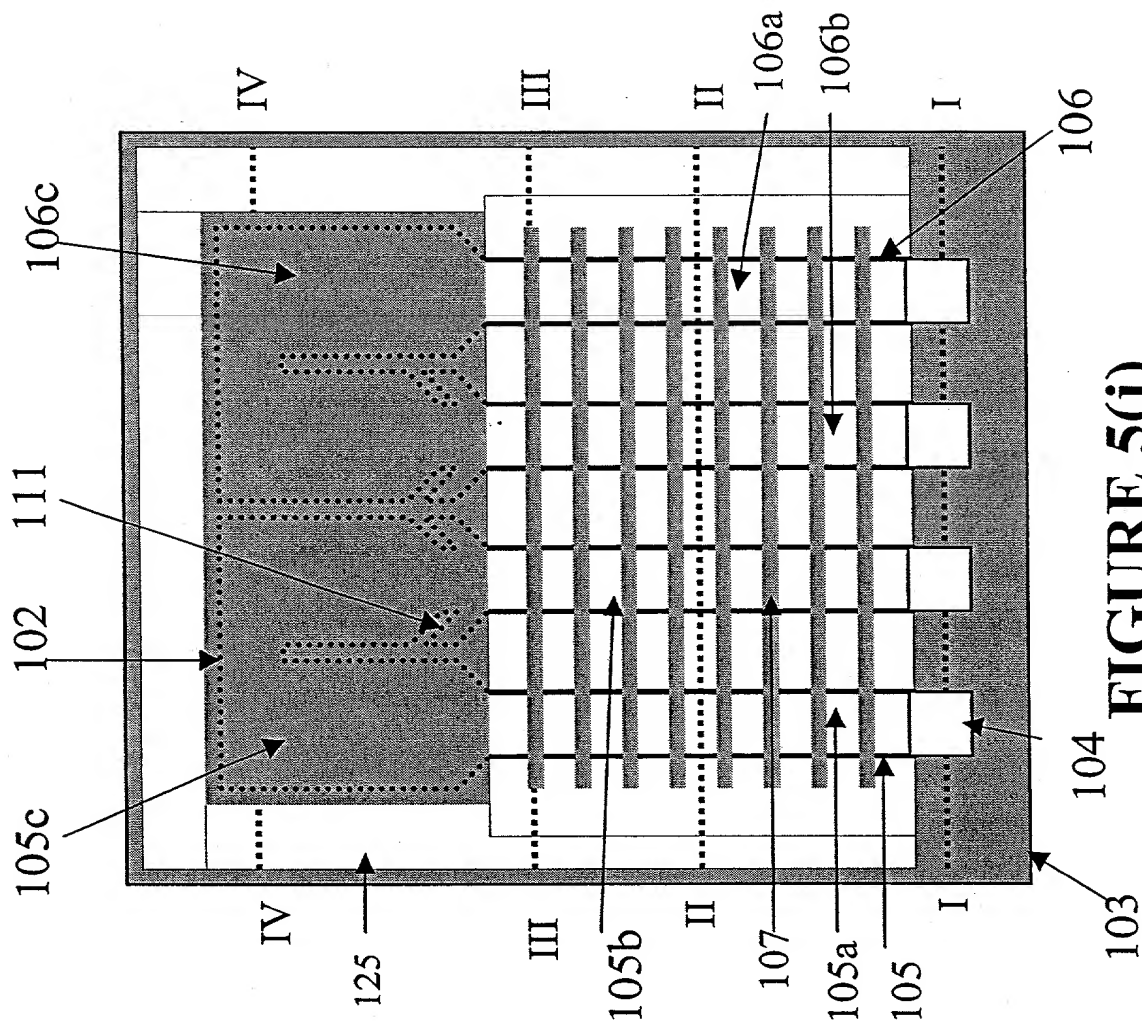


FIGURE 5(j)

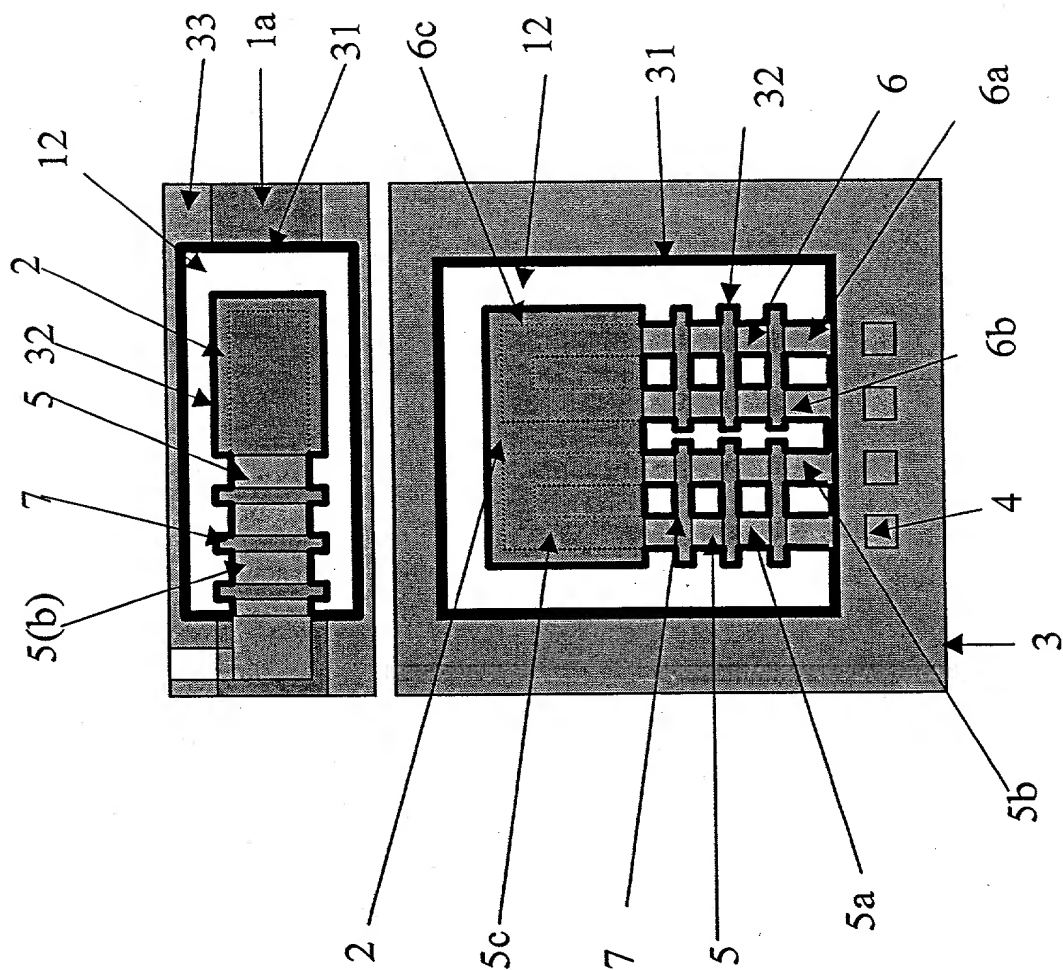


FIG. 7 is a perspective view of the device 100, showing the front face 102, the top face 104, and the side face 106. The device 100 is a rectangular block with a central slot 108. The front face 102 is the face closest to the viewer, the top face 104 is the face at the top, and the side face 106 is the face on the right. The central slot 108 is a rectangular opening in the front face 102.

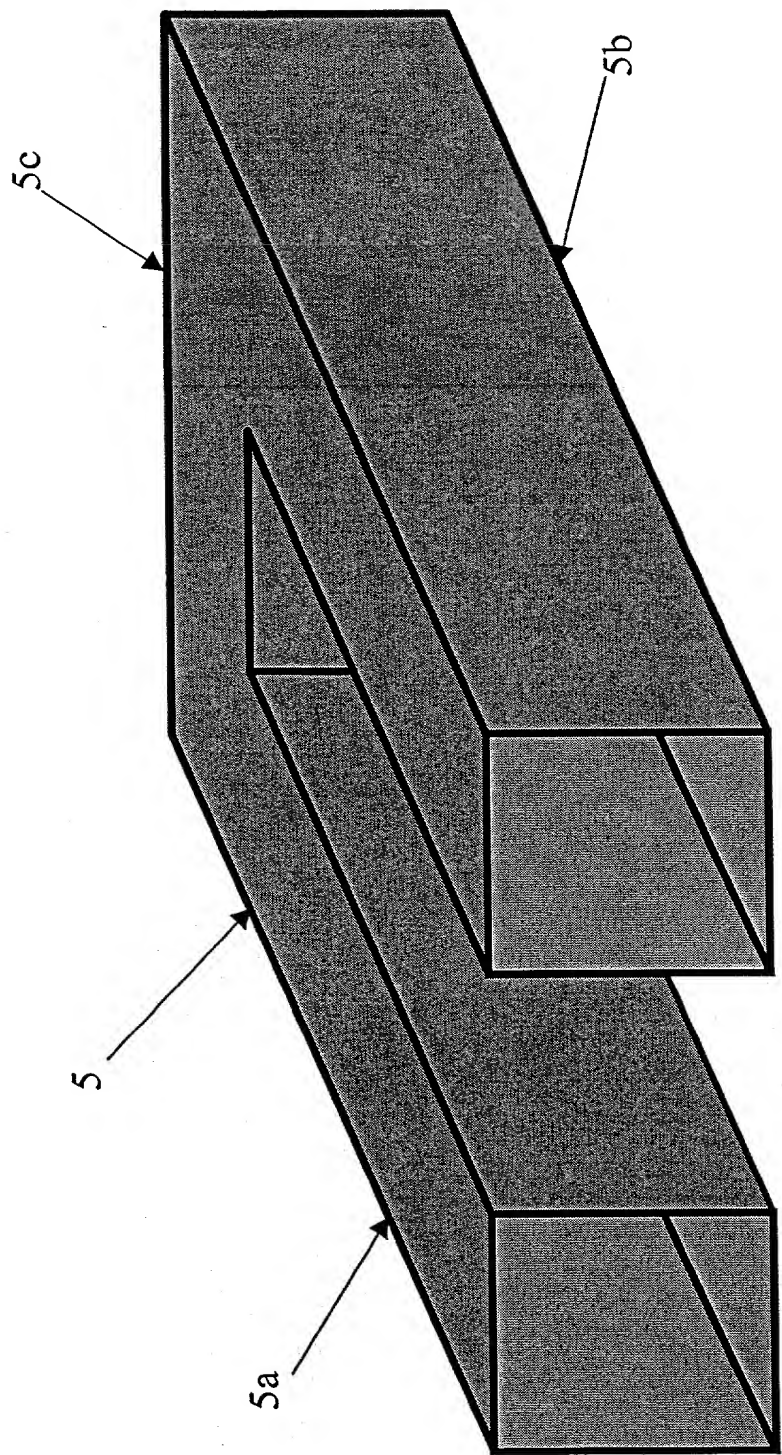
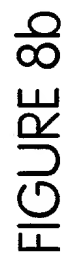
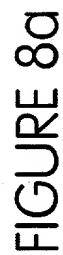
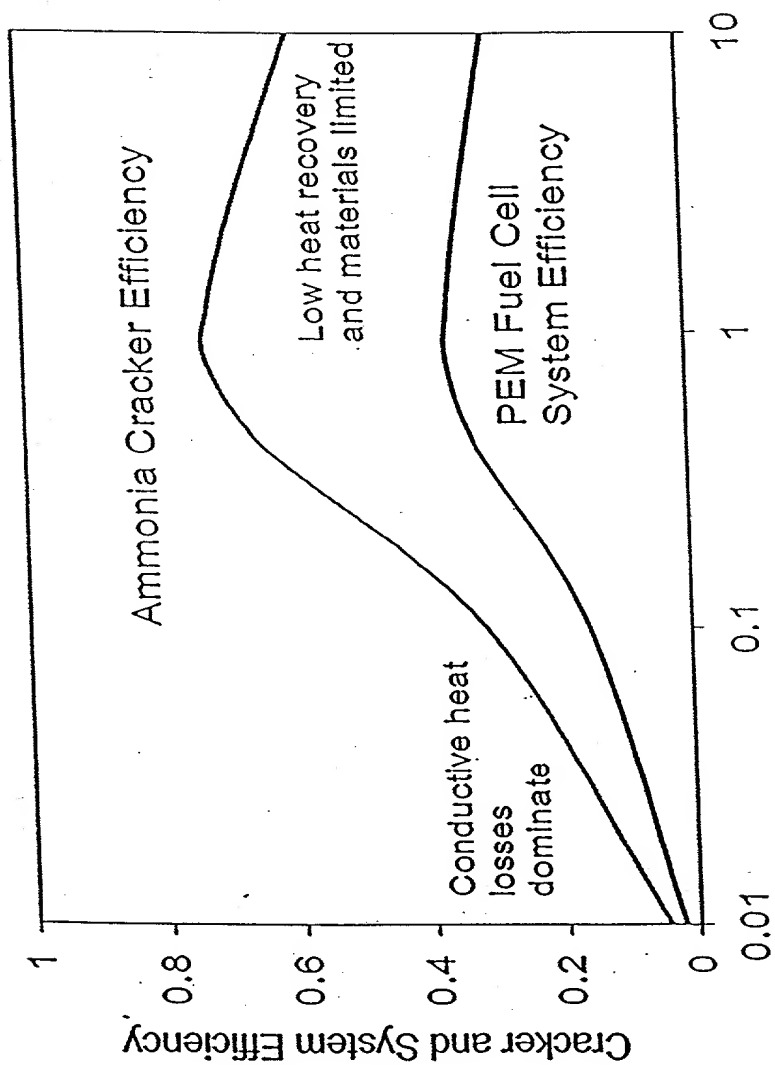


FIGURE 7





System Power Output (w)

FIGURE 9

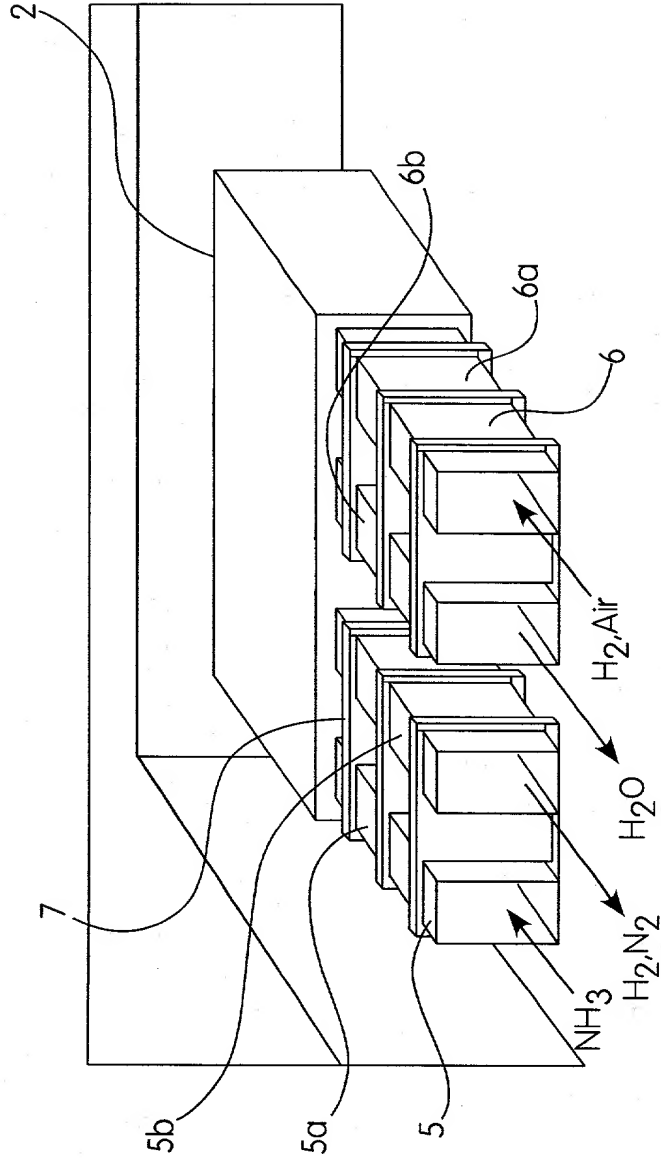


FIGURE 10a

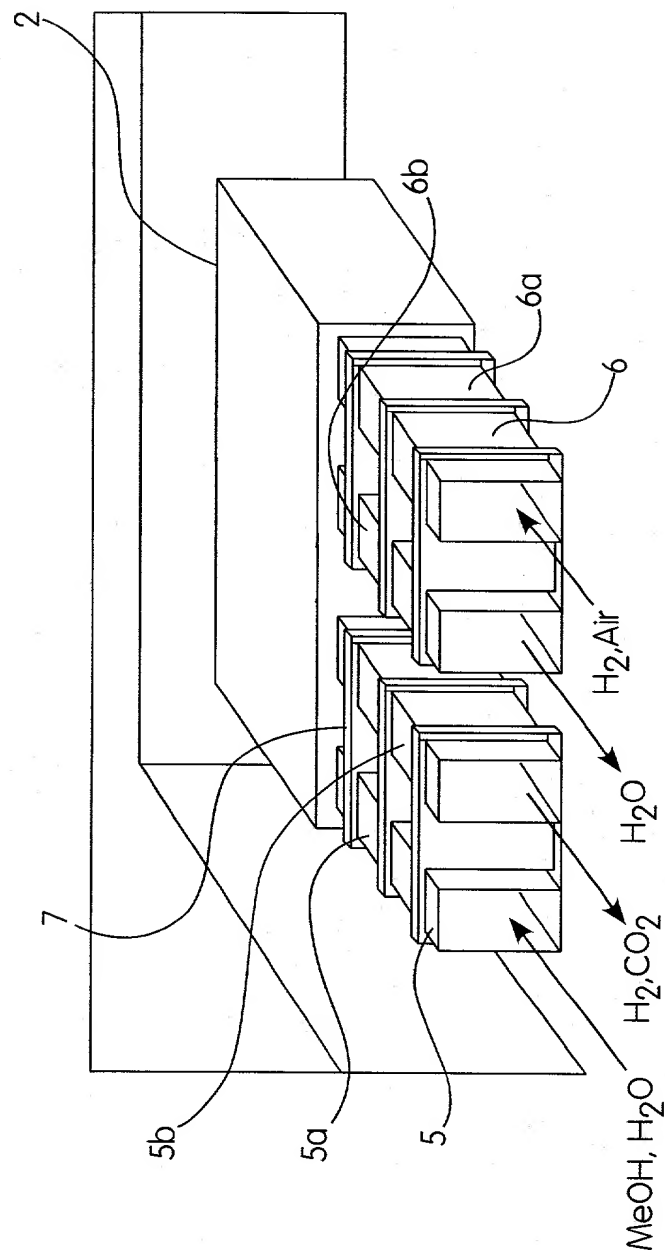


FIGURE 10b

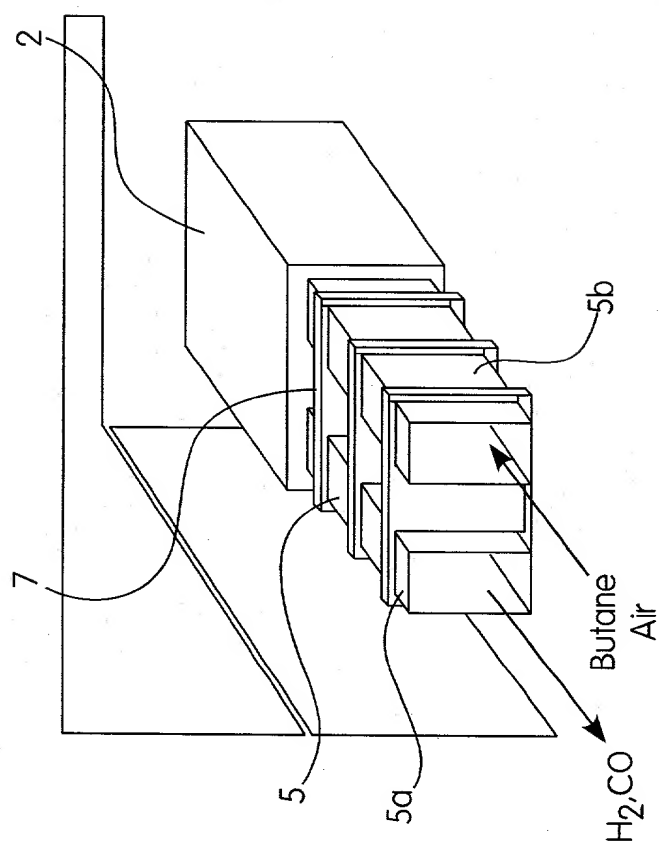


FIGURE 10c

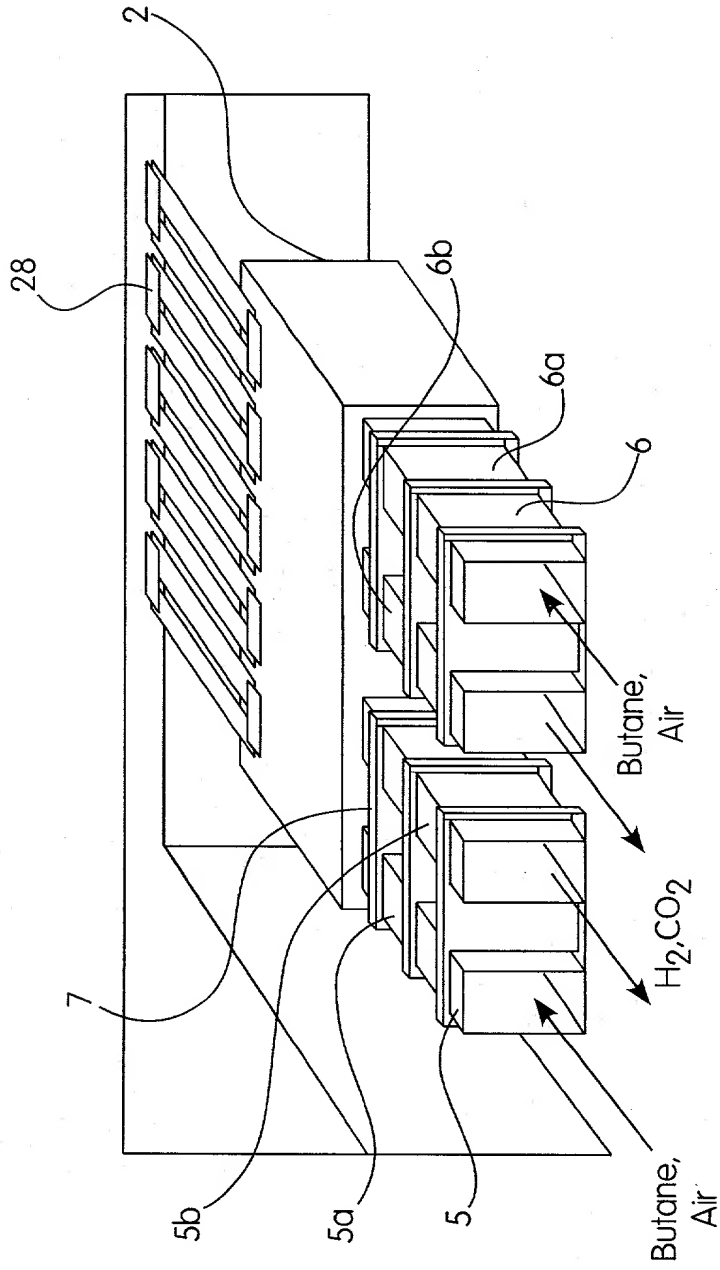


FIGURE 10d

FIGURE 11

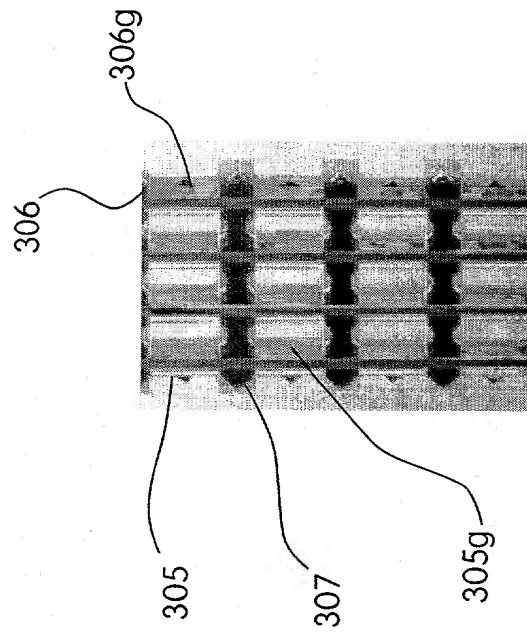


FIGURE 12a

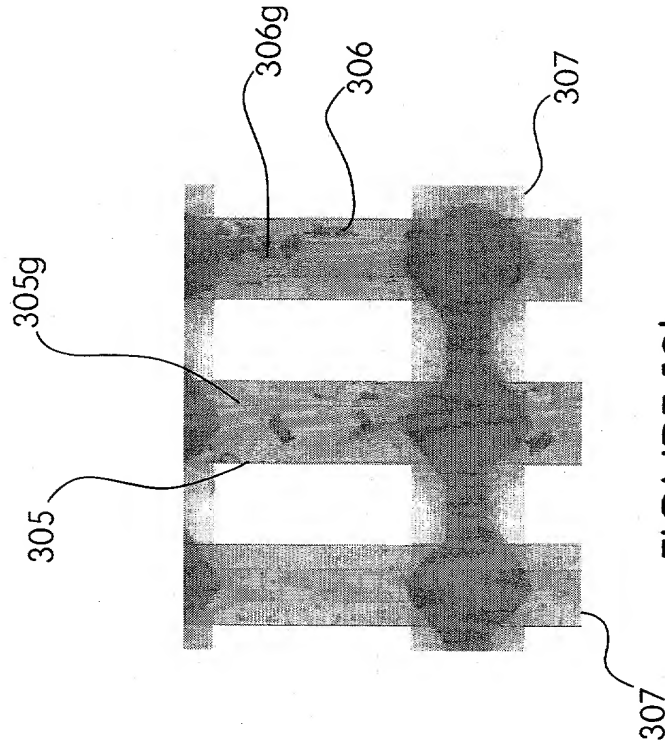


FIGURE 12b

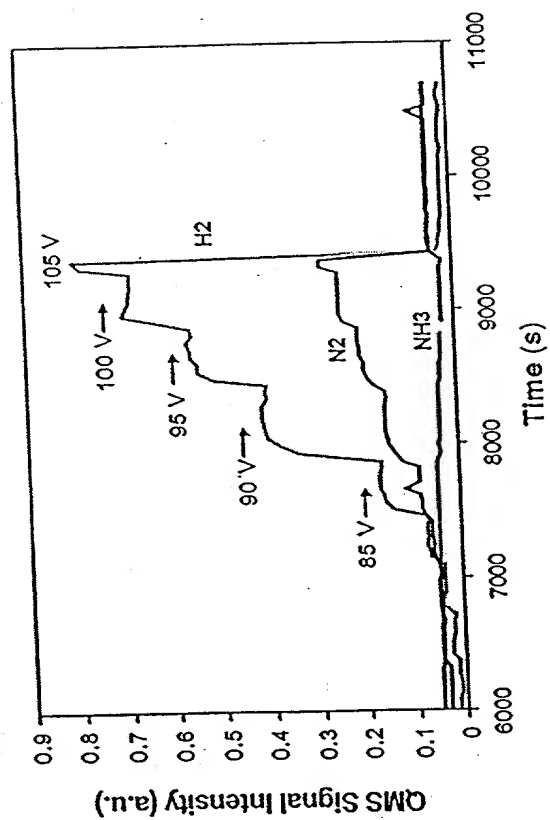


FIGURE 12(c)

